Integrated Device Technology, Inc.

64K x 8
64K x 9
CMOS STATIC RAM MODULE

IDT7M812
IDT7M912

FEATURES:

- High-density 512K CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - — Military: 25ns (max.)
  - — Commercial: 15ns (max.)
- Low power consumption
  - — Active: 2.4W (typ. in 64K x 8 organization)
  - — Standby: 240µW (typ. in 64K x 8 organization)
- Available in 40–pin, 600 mil center sidebraze DIP
- Single 5V (±10%) power supply
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL– compatible

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K high-speed CMOS static RAMs constructed on a multi-layered co-fired ceramic substrate using 8 IDT7187 (64K x 1) static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds can be achieved by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

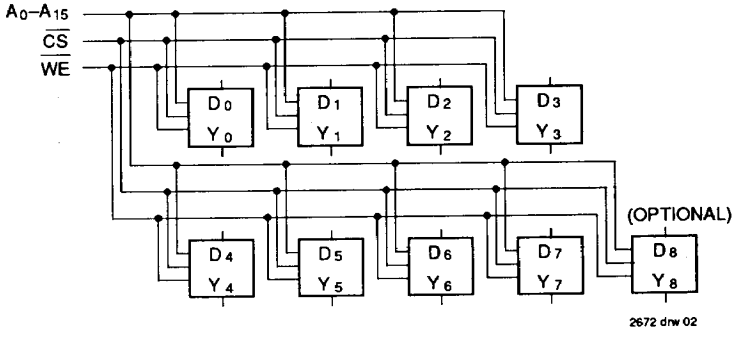
The IDT7M812/IDT7M912 are available with maximum access times as fast as 15ns commercial and 25ns military temperature ranges, with maximum operating power consumption of only 8.9W (IDT7M912, 25ns, 64K x 9 option). The module also offers a standby power mode of 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL–compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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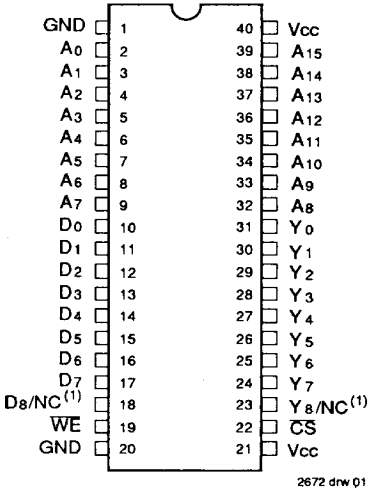
PIN CONFIGURATION (1, 2)



2672 drw 01

TOP VIEW
DIP

NOTES:
1. For the IDT7M912 (64K x 9 version)Pin 18 and Pin 23 are D8 and Y8 respectively. For the IDT7M812 (64K x 8 version), these pins are No Connects.
2. For module dimensions, please refer to drawing M9 and M10 in the packaging section.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commerical	0°C to +70°C	0V	5.0V ± 10%

2672 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
1. VIL = –3.0V for pulse width less than 20ns.

2672 tbl 03

PIN NAMES

A0–A15	Address
D0–D8	Data Input
Y0–Y8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
NC	No Connect

2672 tbl 08

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2672 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2672 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	7M812(2)	7M912(2)	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	12	12	pF
CIN(A)	Input Capacitance (Address)	VIN = 0V	72	80	pF
CIN(C)	Input Capacitance ($\overline{CS}$, $\overline{WE}$)	VIN = 0V	72	80	pF
COUT	Output Capacitance	VOUT = 0V	12	12	pF

NOTES:

2672 tbl 07

1. This parameter is guaranteed by design but not tested.
2. Maximum rated values

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = –55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min.; I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min.; I_{OH} = –4mA	2.4	—	V

2672 tbl 09

Symbol	Parameter	Test Conditions	IDT7M812				IDT7M912				Unit
			Min.	Typ.(1)	Max.(3)	Max.(2)	Min.	Typ.(1)	Max.(3)	Max.(2)	
I_{CC1}	Operating Current	f = 0; $\overline{CS}$ = V_{IL}, V_{CC} = Max.; Output Open	—	520	1080	1120	—	580	1215	1260	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	—	520	1440	1400	—	580	1620	1575	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	280	520	520	—	310	585	585	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; V_{IN} > V_{CC} – 0.2V or < 0.2V	—	0.1	200	200	—	0.4	225	225	mA

2672 tbl 04

NOTES:
1. V_{CC} = 5.0V, T_A = +25°C.
2. t_{AA} = 20, 25, 30, 35, 45, 55, 65ns.
3. t_{AA} = 15ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2672 tbl 10

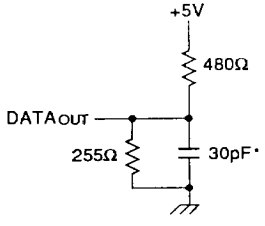


Figure 1. Output Load

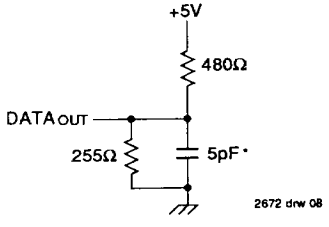


Figure 2. Output Load
(for t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW})

* Including scope and jig.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C and 0° to +70°C)

Symbol	Parameter	7M812S15 7M912S15 (Com'l. Only)		7M812S20 7M912S20 (Com'l. Only)		7M812S25 7M912S25		7M812S30 7M912S30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	30	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{OLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Chip Deselect to Output in High Z	—	6	—	6	—	20	—	25	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	30	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	12	—	15	—	23	—	28	—	ns
t_{AW}	Address Valid to End of Write	12	—	15	—	23	—	28	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	3	—	3	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	8	0	20	0	25	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS (Cont'd.)

(V_{CC} = 5V ±10%, T_A = –55°C to +125°C and 0° to +70°C)

Symbol	Parameter	7M812S35 7M912S35		7M812S45 7M912S45		7M812S55 7M912S55		7M812S65 7M912S65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	65	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	65	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	65	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{OLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	30	—	30	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	35	—	35	—	35	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	65	—	ns
t_{CW}	Chip Select to End of Write	35	—	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	35	—	40	—	50	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	30	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	25	—	30	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	0	25	0	30	0	30	0	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

2672 tbl 05

NOTE:
1. This parameter is guaranteed by design, but not tested.

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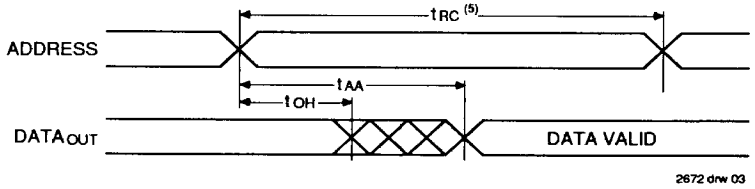
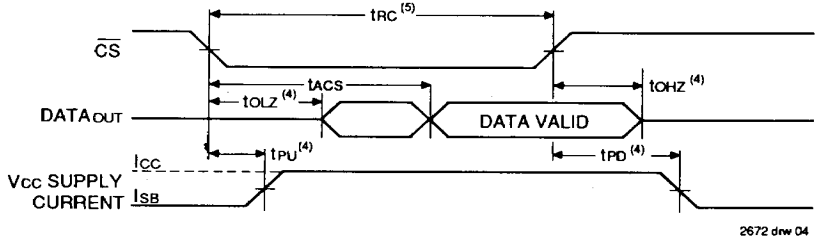
TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)

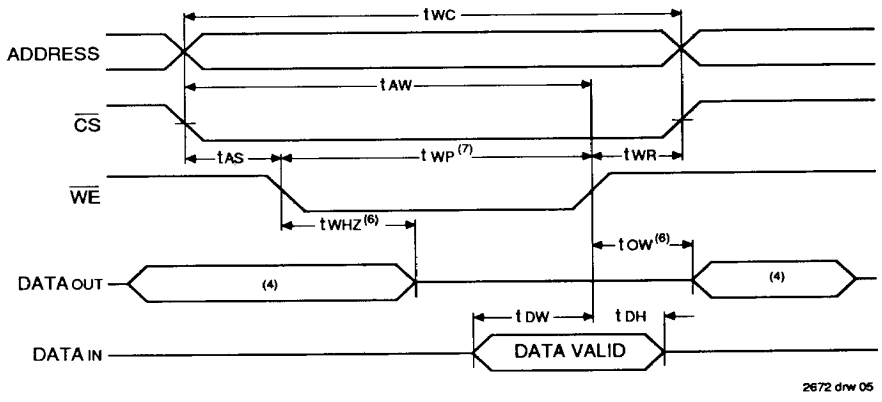


TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)

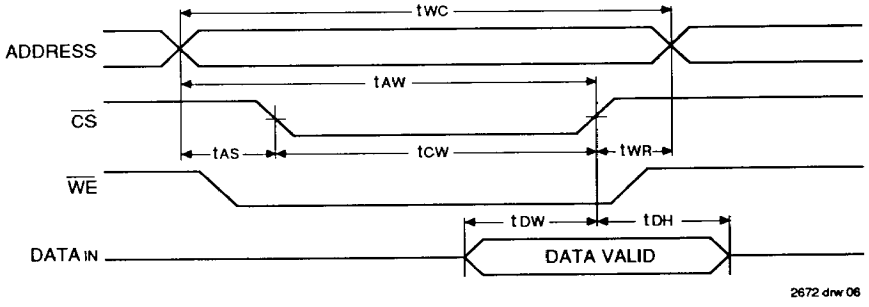


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is guaranteed by design, but not tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transactions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.

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ORDERING INFORMATION